Mentor Graphics

2nd Training Program on Verification of Electronic Design and Systems using System Verilog

2010 Batch

Program Details

Venue : Mentor Graphics (India) Pvt. Ltd., Building A, Plot # 5, Sector-127 Noida
Timings **:** 10 AM to 6 PM (Lunch Provided)
Date **:** August 16 – October 10, 2010

As part of our Higher Education Program, Mentor Graphics Noida (a Corporate R&D Center of Mentor Graphics Corporation) conducted training on "Verification of Electronic Design and Systems using SystemVerilog" in 2009 and was well received by the 30 selected students. The 8 week training was attended by 30 selected students from colleges in Delhi NCR and North India. The training gave them an insight of the EDA Industry and helped them get a headstart in their career. Some testimonials of the students who attended the training program and other statistics are available at www.mentor.com/india .

Continuing with our initiative to help students become proficient in leading edge EDA tools, Mentor Graphics Noida, is pleased to announce the **2nd** "**Verification of Electronic Design and Systems using SystemVerilog**" training program in 2010. This training program is available for students who have graduated from colleges in Delhi NCR and North India and **who have not yet found placement**. The program will be for **eight weeks** beginning **August 16th – October 10, 2010** from 10am to 6pm (Monday to Friday). Industry professionals and Experts will deliver this program using SystemVerilog Hardware Verification Language constructs and OVM methodology. The program will include extensive labs using Mentor Tools and will also include some projects.

Eligibility

- **B.Tech or B.E. degree graduates in Electronics, Computer Science and Electrical are eligible with a CGPA of 7 and above.**
- **The candidate should not be employed in any company at the time of the training.**

Selection Process

- Please visit www.mentor.com/india for online submission (statement of purpose and biodata). We will accept entries till July 23, 2010.
- Short listing will be based on a "Statement of Purpose" (limited to 500 characters) as to why you would want to take this program.
- Preferable CGPA of 7 & above.

- Short-listed candidates will be called for a written test. (aptitude/analytical) in order to qualify for the program. The written test will be held at Mentor Graphics, Noida office on July 31, 2010.

- Results of the final selected candidates will be announced on August 6, 2010.

- Mentor Graphics will select approximately a total of 30 candidates from all institutes.

- Mentor Graphics selection decision will be final.

- For further queries please write to noidahep_training@mentor.com

The Key Modules of the program are:

- Introduction to Logic Design and Verification (Block level and System Level)
- Introduction to SystemVerilog as a Verification Language
- Introduction to SystemVerilog Open Verification Methodology
- Concepts of Verification Management and Coverage using Questa Verification environment

This program is available **free of cost**. An application form for this program is available at http://www.mentor.com/india/eduservices/india-hep-course Interested students should fill up this form and submit it online latest by **July 23, 2010**. **Short-listed applicants will be called for a written (aptitude/analytical) test in our office on July 31, 2010**. A total of 30 students will be selected for this program. **Selected applicants will be informed by August 6, 2010.**

Best Wishes

Prof. (Dr.) Ajay Rana
Director