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A Novel Approach for High Speed and low Power by using VLSI Domino Circuits

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***Abstract*-As technology scales down beyond sub 22nm regime shorter channel effect dominate, single gate MOSFET face great challenge in nanometer while scaling which results in exponential increase in sub-threshold and gate oxide leakage current. To overcome non- planer CMOS device with multi gate technique is adopted to increase the performance and lesser area benefits. Double gate FinFET Technology have excellent control over the thin silicon fins with two electrically coupled gates by mitigate all the limitations that occurs in CMOS. In this paper Domino logic circuit with wide fan-in OR in simulated in FinFET technology by BISM4 model using HSPICE at 45nm and 32nm process technology. Double gated circuit technique at 45nm reduces the delay by 89.6%, power by 27% and leakage current by 42.57% and 25.86% for 0 and 1 input respectively. Same at 32nm reduces the delay by 90.23%, power by 22% and leakage current by 21.33% and 11.06% for 0 and 1 input respectively.**

***Keywords*-FinFET, High Speed, shorter channel effect, Multigate device.**

I. INTRODUCTION

Silicon based CMOS technology emerges from last 25 years in microelectronics industries. According to the Moore law transistor has to double in same area in every two years. Scaling of CMOS technology is to improve the device density and performance of the circuit. Difficulties in shrinking of device dimension of traditional bulk CMOS have promoted to develop a new architecture with double gate which have higher scalability than single gate transistor, since both the gate control the fin potential over the body [1]. The two electrically coupled gates and thin silicon body suppress the shorted channel effect in sub 22nm and beyond, double gate FinFET thus reduces the sub threshold and gate oxide leakage current [2]. Enhance the control over the gate reduces shorter channel effect thick gate oxide in double gate as compare to single gate to reduces gate oxide tunnelling current significantly. The fin body of a double-gate device is typically undoped or lightly doped, therefore enhancement of the carrier mobility and the device variations due to doping fluctuations are reduced in a double-gate FinFETas compared to a single-gate MOSFET. The main differences exist between FinFET and bulk-CMOS appears when larger device are required.

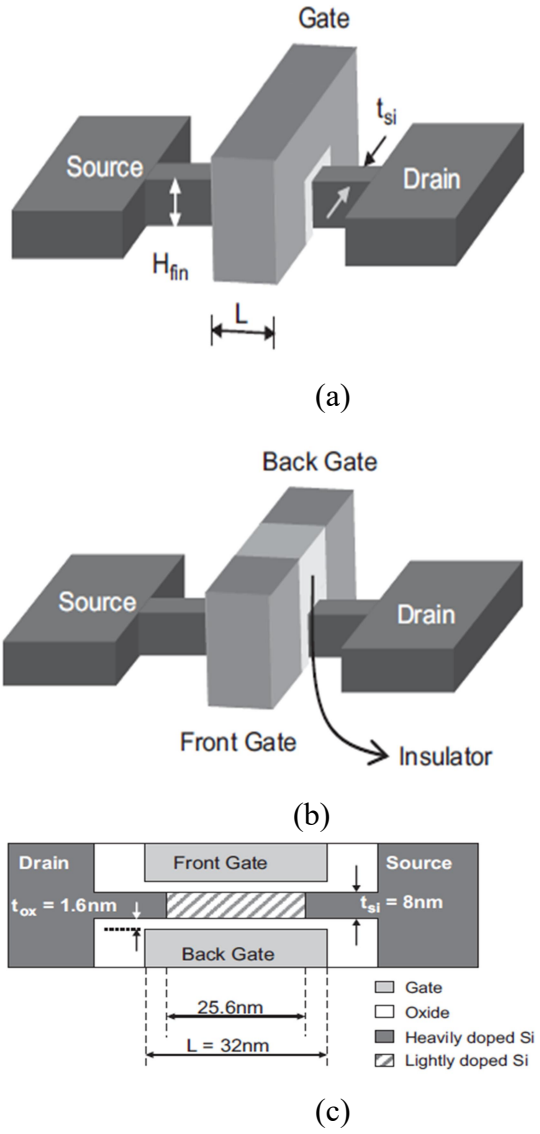

Fig.1. The device architectures of FinFETs. (a) 3D structure of a one-fin tied-gate FinFET. (b) 3D structure of a one-fin independent-gate FinFET. (c) Cross-sectional top view of a FinFET with a drawn channel length of 32 nm.

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II. FINFET TECHNOLOGY

The main advantage of the FinFET structure is that fabrication of double gate by using a single lithography and etch step, gate is easily wrapped over the silicon fin, Front gate and back gate have different doping profile, so both the gate operate independently according to the requirement [3]. One of the main challenges while making of FinFET over bulk-CMOS it has high current drive by reducing parasitic resistance. Source drain region requires re-engineering.

III. Literature Review

Domino logic circuit is basically used in high speed microprocessors, where speed and high performance is the prime concern with scaling of technology.

Footless Domino Logic Circuit

Footless domino logic circuit is an old domino logic circuit. The major difference is that, in footless domino logic circuit is that the footed NMOS transistor which is placed in the circuit like footed domino logic circuit is absent in footless domino logic circuit. The circuit diagram for footless domino logic circuit can be given as shown in Fig. 2.

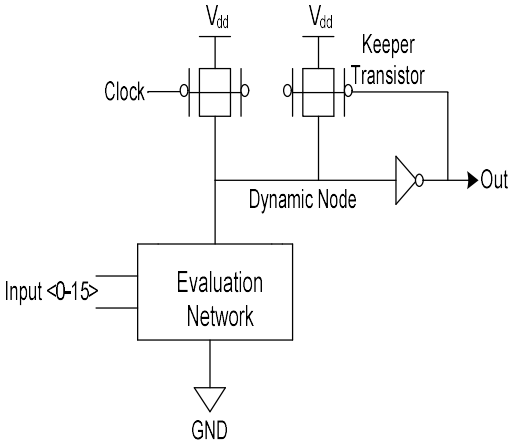

Fig. 2. Footless domino logic circuit

A. Footed Domino Logic Circuit

Footed domino logic is a general form of domino logic circuit. It is so called because of a footer transistor is placed in the circuit. The footer transistor is generally an NMOS transistor. Footer transistor shows a better noise and leakage tolerance because of leakage reduction due to stacking effect [4][5]. The circuit diagram for footed domino logic circuit can be given as shown in Fig. 3.

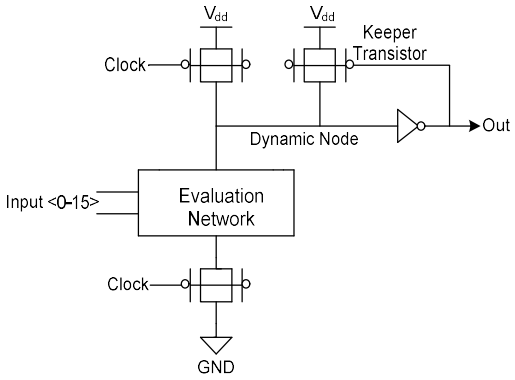

Fig. 3. Footed domino logic circuit

B. High speed Domino Logic Circuit

High speed domino is another domino logic circuit. In domino logic circuit current drawn through the keeper transistor and pull down network NMOS transistors at the beginning of the evaluation phase, can be reduced by applying a clock delay in the circuit [6]. That does not affect the leakage current in the circuit. But apart from this the extra clock delay consumes extra area and power, which is a big drawback of the circuit. It gives an effective solution to increase the robustness of the circuit [7]-[11].

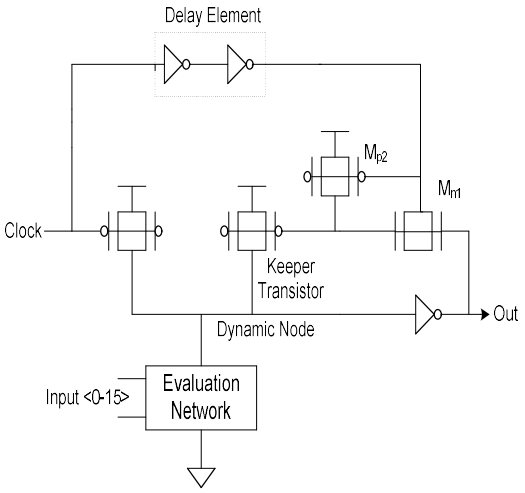

Fig. 4. High speed domino logic circuit

In High speed domino logic circuit when clock becomes high, M_{n1} is still off and M_{p2} is still on. Therefore M_{p2} turns off the keeper transistor. After some delay of inverter M_{p2} becomes off. Now if dynamic node remains high during the evaluation

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phase, NMOS is turn on which turns on the keeper transistor. Hence at the beginning of evaluation phase dynamic node is afloat, so in the absence of keeper transistor, evaluation node may be discharged for any noise at the input section. Also the voltage at the gate of the keeper transistor would be V_{DD}-V_{tMn1}. This would provide a dc current flow through the PMOS keeper transistor and the NMOS network.

C. Conditional keeper Domino Logic Circuit

In most of the high speed timing performance schemes, just before or close to the start of the evaluation phase, the input signals of the dynamic logic gates are ready. In such situations the maximum time slot for any output transition is only a fraction of total evaluation time, which takes half time period of 50% duty cycle clock. Therefore at the output of the gate leakage and noise exists for a long time unnecessarily [12]. In the conventional circuit a standard keeper transistor is used. This standard keeper transistor is turned on unconditionally at the start of the evaluation phase, which takes down the performance of the dynamic logic gate.

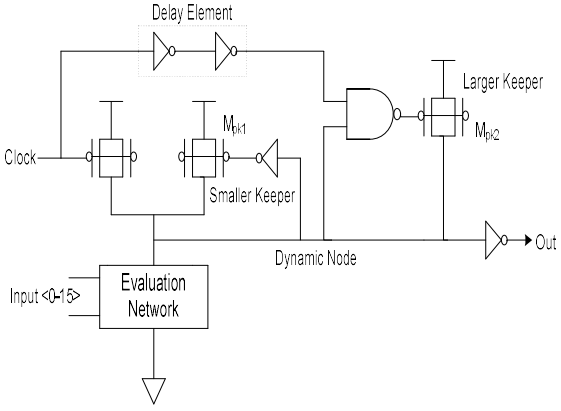

Fig. 5. Conditional keeper domino logic circuit

The conditional keeper domino logic contains two PMOS transistor keeper circuit having variable strength. One keeper transistor is of smaller strength and other is of higher strength. The circuit diagram for Conditional keeper is given in Fig. 5.

When the dynamic node is at high voltage M_{kp1} gets turn on to avoid voltage drop at the dynamic node. If the dynamic node is still high, then after a certain amount of delay, during the evaluation phase output of NAND gate becomes low this makes Mkp2 to turn on. For maintaining the state of dynamic node, is M_{kp1} responsible during the beginning of evaluation phase and M_{kp2} is responsible for the rest of the evaluation phase.

IV. PROPOSED CIRCUIT

In this paper, we have done modification over the keeper transistor, which is week keeper for reduction of contention between keeper and evaluation network, we split the keeper transistor into two keeper transistor for proper strength and by sizing of the keeper transistor we reduces the power and delay of the domino circuit.

As shown in Fig. 6, we use Ultra low power stacked design (ULSD) which is the combination of one PMOS and NMOS. ULSD reduces the leakage current compare to other standard logic

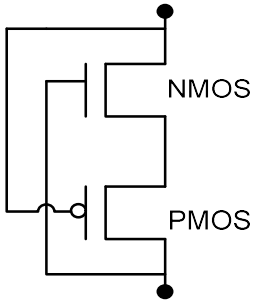

Fig. 6. ULSD

Proposed circuit work in two phase when clock pulse is 0 it is in pre-charge phase, which charge the dynamic node output of the logic is always 0.

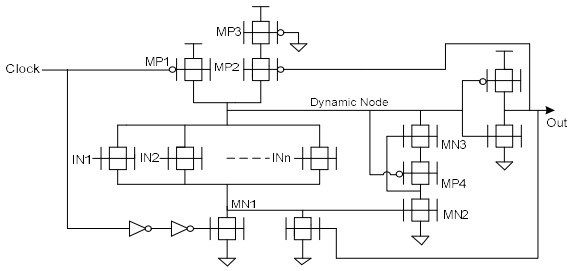

Fig. 7. Simulation and Results discussion

Simulation results is obtained by using BISM4, HSPICE model at 32nm FinFET technology, circuit is simulated in SP & LP mode with .8v supply at 100MHz frequency, operating temperature is 27^0c with C_L=1fF for 8 and 16 input OR gate.

TABLE I. Calculation of Average power, Delay and PDP for8 input OR gate in SP and LP mode using FinFET technology

	Average Power		Delay		PDP	
	SP Mode	LP Mode	SP Mode	LP Mode	SP Mode	LP Mode
FLD	0.1200	0.03164	9.635	8.2431	1.1562	0.2608
FDL	0.0776	0.02421	15.58	13.452	0.4929	0.0119
HSD	0.1306	0.03324	9.1855	7.982	1.1996	0.3987
CKD	0.1537	0.0428	10.32	9.541	1.5861	0.4083
Proposed Circuit	0.1062	0.0280	7.292	7.156	0.7744	0.0216

TABLE II. Calculation of Average power, Delay and PDP for16 input OR gate in SP and LP mode using FinFET technology

	Average Power		Delay		PDP	
	SP Mode	LP Mode	SP Mode	LP Mode	SP Mode	LP Mode
FLD	0.14277	0.03891	10.235	9.3714	1.4612	0.3646
FDL	0.09602	0.02781	19.9445	15.341	1.9146	0.4266
HSD	0.15794	0.03916	10.02	9.2541	1.4609	0.3623
CKD	0.18371	0.04943	11.0185	10.253	1.8835	0.5068
Proposed Circuit	0.1262	0.03265	8.384	8.9451	1.0580	0.2737

V. CONCLUSION

In this paper we have studied various domino topologies for low power and high speed VLSI design. Compare to the CMOS domino logic, proposed FinFET domino logic circuit shows sever improvement in power reduction and improve the performance. Moreover, due to higher I_{ON}/I_{OFF} ratio and faster switching speed, improvement in FinFET technology improves the limiting frequency of the domino logic circuit. The existing and proposed circuit performance has been evaluated by HSPICE using a BSIM4 32nm CMOS and FinFET technology, power supply of .8V for 8 and 16 inputs for wide fan-in OR gate. Increasing of W/L ratio of transistor enhance the power consumption, reduces the delay and PDP of overall circuit with different keeper ratio of the domino logic circuit.

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